CLAIMS

What is claimed is:

1. A method for adjusting an output driver, the method comprising the steps of:

receiving a first signal;

applying the first signal to a first tuning element to generate a reference signal;

receiving a second signal;

applying the second signal to a second tuning element to generate a test signal, wherein the second tuning element is configured similarly to the first tuning element;

sampling the reference signal to generate a time-sampled reference signal;

sampling the test signal to generate a time-sampled test signal;

integrating the time-sampled reference signal and the time-sampled test signal to generate an error signal; and

applying the error signal to adjust an output driver.

2. The method of claim 1, wherein receiving a first signal comprises receiving a clock signal.

3. The method of claim 2, wherein the clock signal comprises a frequency of greater than 100MHz.

4. The method of claim 1, wherein applying the first signal to a first tuning element comprises reflecting the first signal towards a source of the first signal.

5. The method of claim 4, wherein reflecting the first signal towards the source results in the reflected signal arriving at the source when a first half of the first signal has completed exiting the source.

6. The method of claim 1, wherein receiving a second signal comprises enabling reflections generated by a signal transition of the second signal and reflected by the second tuning element to damp out before a subsequent signal transition of the second signal.

7. The method of claim 1, wherein integrating the time-sampled reference signal and the time-sampled test signal comprises applying the signals to a feedback loop.

8. A system, comprising:

a reference driver coupled to a first tuning element, the reference driver and the first tuning element configured to receive a first input signal and generate a reference signal comprising a primary reference component and a reflected reference component;

a test driver coupled to a second tuning element, the test driver and the second tuning element configured to receive a second input signal and generate a test signal comprising a primary test component and a reflected test component;

an integrator configured to receive the reference signal and the test signal and generate an error signal.

9. The system of claim 8, wherein the first tuning element comprises a first transmission line.

10. The system of claim 9, wherein the first printed circuit board trace has an input end coupled to an output of the reference driver and a length that generates the reflected reference component such that the reflected reference component reaches the output of the reference driver in synchronization with the primary reference component.

11. The system of claim 10, wherein the first transmission line has an output end that is electrically open.

12. The system of claim 8, wherein the second tuning element comprises a second transmission line.

13. The system of claim 11, wherein the second transmission line has an input end coupled to an output of the test driver and a length substantially equal to that of the first transmission line.

14. The system of claim 13, wherein the second transmission line has an output end that is electrically open.

15. The system of claim 8, further comprising:

a delay element configured to receive the second input signal and generate a control signal;

a first sample and hold circuit coupled between the reference driver and the integrator, the first sample and hold circuit configured to generate a time-sampled reference signal in response to the control signal; and

a second sample and hold circuit coupled between the test driver and the integrator, the second sample and hold circuit configured to generate a time-sampled test signal in response to the control signal.

16. The system of claim 8, wherein the first input signal comprises a clock signal.

17. The system of claim 16, wherein the clock signal comprises a frequency of greater than 100MHz.

18. A system for adjusting an output driver to reduce the effect of impedance mismatches between signal sources and signal traces, comprising:

means for generating a reference signal responsive to a first input signal, wherein the reference signal emulates signal reflections due to a characteristic impedance of transmission lines in the system;

means for generating a test signal responsive to a second input signal that enables signal reflections responsive to second input signal transitions and the characteristic impedance of transmission lines in the system to dampen before subsequent second input signal transitions; and

means for generating an error signal responsive to the reference signal and the test signal.

19. The system of claim 18, further comprising:

means for sampling the reference signal; and

means for sampling the test signal.

20. The system of claim 18, wherein the means for generating an error signal comprises means for integrating the reference signal and the test signal.